**Experiment no: 11 Date:**

**BINARY COUNTER**

**AIM:**

To write a verilog HDL program for binary counter and verify its output.

**SOFTWARE REQUIRED:**

Xilinx ISE 10.1

**ALGORITHM:**

Step1: Define the specifications and initialize the design. Step2: Write the source code in VERILOG.

Step3: Check the syntax and perform synthesis .

Step4: Write different combinations of input using the test bench. Step5:Verify the output by simulating the source code.

**VERILOG SOURCE CODE:**

module counter ( input clk,

input rstn,

output reg[3:0] out);

always @ (posedge clk) begin

if (rstn <= 0)

out <= 0;

else

out <= out + 1;

end

endmodule

**TESTBENCH:**

module tb\_counter;

reg clk;

reg rstn;

wire [3:0] out;

counter uut(clk,rstn,out);

always #5 clk = ~clk;

// This initial block forms the stimulus of the testbench

initial

begin

clk <= 0;

rstn <= 0;

#20

rstn <= 1;

#80

rstn <= 0;

#50

rstn <= 1;

#200

$finish;

end

initial begin

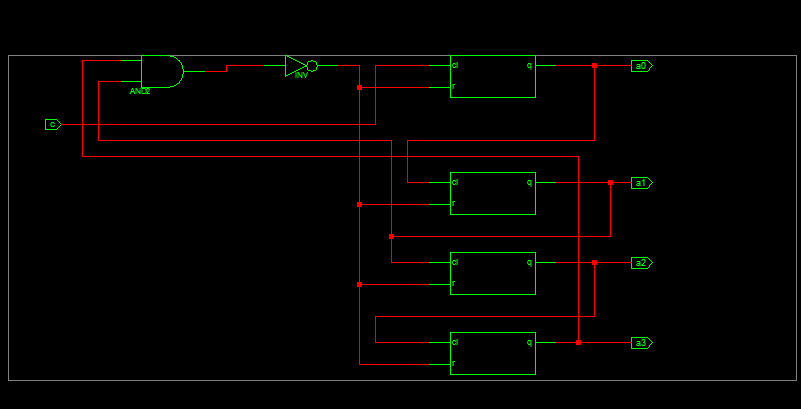
$dumpvars(0,uut);

$dumpfile("dump.vcd");

end

endmodule

**RTL SCHEMATIC:**



**SYNTHESIS REPORT:**

\* Final Report \*

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Final Results

RTL Top Level Output File Name : count1.ngr Top Level Output File Name : count1 Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs 6

Cell Usage :

# BELS 6

# INV 1

|  |  |  |
| --- | --- | --- |
| #  # | LUT2  LUT2\_L | : 1  : 1 |
| # | LUT3 | : 1 |
| # | LUT4 | : 2 |

# FlipFlops/Latches 4

# FDR 4

# Clock Buffers 1

# BUFGP 1

# IO Buffers 5

# IBUF 1

# OBUF 4

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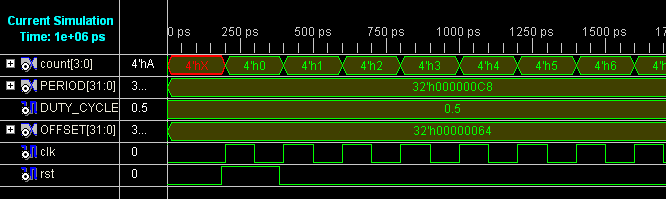
Device utilization summary:

Selected Device : 3s100evq100-4

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Number of Slices: | 3 | out of | 960 | 0% |
| Number of Slice Flip Flops: | 4 | out of | 1920 | 0% |
| Number of 4 input LUTs: | 6 | out of | 1920 | 0% |
| Number of IOs: | 6 |  |  |  |
| Number of bonded IOBs: | 6 | out of | 66 | 9% |

Number of GCLKs: 1 out of 24 4%

**SIMULATION OUTPUT:**



**RESULT:**

Thus a verilog HDL program was written for binary counter and its output was verified.